NPTEL Video Lecture Topic List - Created by LinuXpert Systems, Chennai

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NPTEL Video Course - Electronics and Communication Engineering - Digital System design with PLDs and FPGAs
Subject Co-ordinator - Prof. Kuruvilla Varghese
Co-ordinating Institute - IISc - Bangalore
Sub-Titles - Available / Unavailable | MP3 Audio Lectures - Available / Unavailable
Lecture 1 - Course Contents, Objective
Lecture 2 - Revision of Prerequisite
Lecture 3 - Design of Synchronous Sequential Circuits
Lecture 4 - Analysis of Synchronous Sequential Circuits
Lecture 5 - Top-down Design
Lecture 6 - Controller Design
Lecture 7 - Control algorithm and State diagram
Lecture 8 - Case study 1
Lecture 9 - FSM issues 1
Lecture 10 - FSM Issues 2
Lecture 11 - FSM Issues 3
Lecture 12 - FSM Issues 4
Lecture 13 - FSM Issues 5
Lecture 14 - Synchronization 1
Lecture 15 - Synchronization 2
Lecture 16 - Case study 2
Lecture 17 - Case study on FPGA Board
Lecture 18 - Entity, Architecture and Operators
Lecture 19 - Concurrency, Data flow and Behavioural models
Lecture 20 - Structural Model, Simulation
Lecture 21 - Simulating Concurrency
Lecture 22 - Classes and Data types
Lecture 23 - Concurrent statements and Sequential statements
Lecture 24 - Sequential statements and Loops
Lecture 25 - Modelling flip-flops, Registers
Lecture 26 - Synthesis of Sequential circuits
Lecture 27 - Libraries and Packages
Lecture 28 - Operators, Delay modelling
Lecture 29 - Delay modelling
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Lecture 30 - VHDL Examples

Lecture 31 - VHDL coding of FSM

Lecture 32 - VHDL Test bench

Lecture 33 - VHDL Examples, FSM Clock

Lecture 34 - Evolution of PLDs

Lecture 35 - Simple PLDs

Lecture 36 - Simple PLDs

Lecture 37 - Complex PLDs

Lecture 38 - FPGA Introduction

Lecture 39 - FPGA Interconnection, Design Methodology

Lecture 40 - Xilinx Virtex FPGAâ s CLB

Lecture 41 - Xilinx Virtex Resource Mapping, IO Block

Lecture 42 - Xilinx Virtex Clock Tree

Lecture 43 - FPGA Configuration

Lecture 44 - Altera and Actel FPGAs
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