NPTEL Video Course - Electronics and Communication Engineering - NOC:VLSI Design Verification and Test

Subject Co-ordinator - Dr. Santosh Biswas, Jatindra Kumar Deka, Prof.Arnab sarkar

Co-ordinating Institute - IIT - Guwahati

Sub-Titles - Available / Unavailable | MP3 Audio Lectures - Available / Unavailable

Lecture 1 - Introduction - Part 1
Lecture 2 - Introduction - Part 2
Lecture 3 - Overview of VLSI Design Flow
Lecture 4 - High Level Synthesis Overview - Part 1
Lecture 5 - High Level Synthesis Overview - Part 2
Lecture 6 - Scheduling in HLS - Part 1
Lecture 7 - Scheduling in HLS - Part 2
Lecture 8 - Scheduling in HLS - Part 3
Lecture 9 - Scheduling in HLS - Part 4
Lecture 10 - Scheduling in HLS - Part 5
Lecture 11 - Scheduling in HLS - Part 6
Lecture 12 - Scheduling in HLS - Part 7
Lecture 13 - Resource Sharing and Binding in HLS - Part 1
Lecture 14 - Resource Sharing and Binding in HLS - Part 2
Lecture 15 - Resource Sharing and Binding in HLS - Part 3
Lecture 16 - Resource Sharing and Binding in HLS - Part 4
Lecture 17 - Resource Sharing and Binding in HLS - Part 5
Lecture 18 - Resource Sharing and Binding in HLS - Part 6
Lecture 19 - Resource Sharing and Binding in HLS - Part 7
Lecture 20 - Logic Synthesis - Part 1
Lecture 21 - Logic Synthesis - Part 2
Lecture 22 - Logic Synthesis - Part 3
Lecture 23 - Physical Design - Part 1
Lecture 24 - Physical Design - Part 2
Lecture 25 - Physical Design - Part 3
Lecture 26 - Introduction to formal methods for design verification
Lecture 27 - Temporal Logic
Lecture 28 - Syntax and Semantics of CLT
Lecture 29 - Syntax and semantics of CTL (Continued...)

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Lecture 30 - Equivalences between CTL Formulas
Lecture 31 - Introduction to Model Checking
Lecture 32 - Model checking Algorithms
Lecture 33 - Model checking Algorithms (Continued...)
Lecture 34 - Model Checking with Fairness
Lecture 35 - Binary Decision Diagram
Lecture 36 - Ordered Binary Decision Diagram (OBDD)
Lecture 37 - Operation On OBDD
Lecture 38 - OBDD for State Transition Systems E
Lecture 39 - Symbolic Model Checking
Lecture 40 - Introduction to Digital VLSI Testing
Lecture 41 - Functional and Structural Testing
Lecture 42 - Fault Equivalence
Lecture 43 - Fault Simulation - I
Lecture 44 - Fault Simulation - II
Lecture 45 - Fault Simulation - III
Lecture 46 - Testability Measures (SCOAP)
Lecture 47 - Introduction to Automatic Test Pattern Generation (ATPG) and ATPG Algebras
Lecture 48 - D-Algorithm - I
Lecture 49 - D-Algorithm - II
Lecture 50 - ATPG for Synchronous Sequential Circuits
Lecture 51 - Scan Chain based Sequential Circuit Testing - I
Lecture 52 - Scan Chain based Sequential Circuit Testing - II
Lecture 53 - BIST - I
Lecture 54 - BIST - II
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