

## NPTEL Video Lecture Topic List - Created by LinuXpert Systems, Chennai

NPTEL Video Course - Computer Science and Engineering - NOC:Switching Circuits and Logic Design

Subject Co-ordinator - Prof. Indranil Sengupta

Co-ordinating Institute - IIT - Kharagpur

Sub-Titles - Available / Unavailable | MP3 Audio Lectures - Available / Unavailable

- Lecture 1 - Introduction
- Lecture 2 - Octal and Hexadecimal Number Systems
- Lecture 3 - Signed and Unsigned Binary Number Representation
- Lecture 4 - Binary Addition and Subtraction
- Lecture 5 - BCD and Gray Code Representations
- Lecture 6 - Error Detection and Correction
- Lecture 7 - Logic Gates
- Lecture 8 - Logic Families to Implement Gates
- Lecture 9 - Emerging Technologies - Part I
- Lecture 10 - Emerging Technologies - Part II
- Lecture 11 - Switching Algebra
- Lecture 12 - Algebraic Manipulation
- Lecture 13 - Properties of Switching Functions
- Lecture 14 - Obtaining Canonical Representations of Functions
- Lecture 15 - Functional Completeness
- Lecture 16 - Minimization Using Karnaugh Maps - Part I
- Lecture 17 - Minimization Using Karnaugh Maps - Part II
- Lecture 18 - Minimization Using Karnaugh Maps - Part III
- Lecture 19 - Minimization using Tabular Method - Part I
- Lecture 20 - Minimization using Tabular Method - Part II
- Lecture 21 - Design of Adders - Part I
- Lecture 22 - Design of Adders - Part II
- Lecture 23 - Design of Adders - Part III
- Lecture 24 - Logic Design - Part I
- Lecture 25 - Logic Design - Part II
- Lecture 26 - Logic Design - Part III
- Lecture 27 - Binary Decision Diagrams - Part I
- Lecture 28 - Binary Decision Diagrams - Part II
- Lecture 29 - Logic Design using AND-EXOR Network

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- Lecture 30 - Threshold Logic and Threshold Gates
- Lecture 31 - Latches and Flip-Flops - Part I
- Lecture 32 - Latches and Flip-Flops - Part II
- Lecture 33 - Latches and Flip-Flops - Part III
- Lecture 34 - Clocking and Timing - Part I
- Lecture 35 - Clocking and Timing - Part II
- Lecture 36 - Synthesis of Synchronous Sequential Circuits - Part I
- Lecture 37 - Synthesis of Synchronous Sequential Circuits - Part II
- Lecture 38 - Synthesis of Synchronous Sequential Circuits - Part III
- Lecture 39 - Synthesis of Synchronous Sequential Circuits - Part IV
- Lecture 40 - Minimization of Finite State Machines - Part I
- Lecture 41 - Minimization of Finite State Machines - Part II
- Lecture 42 - Design of Registers - Part I
- Lecture 43 - Design of Registers - Part II
- Lecture 44 - Design of Registers - Part III
- Lecture 45 - Design of Counters - Part I
- Lecture 46 - Design of Counters - Part II
- Lecture 47 - Digital-to-Analog Converter - Part I
- Lecture 48 - Digital-to-Analog Converter - Part II
- Lecture 49 - Analog-to-Digital Converter - Part I
- Lecture 50 - Analog-to-Digital Converter - Part II
- Lecture 51 - Analog-to-Digital Converter - Part III
- Lecture 52 - Asynchronous Sequential Circuits - Part I
- Lecture 53 - Asynchronous Sequential Circuits - Part II
- Lecture 54 - Algorithmic State Machine (ASM Chart
- Lecture 55 - Testing of Digital Circuits
- Lecture 56 - Fault Modeling
- Lecture 57 - Test Pattern Generation
- Lecture 58 - Design for Testability
- Lecture 59 - Built-in Self-Test - Part I
- Lecture 60 - Built-in Self-Test - Part II