

# NPTEL Video Lecture Topic List - Created by LinuXpert Systems, Chennai

NPTEL Video Course - Computer Science and Engineering - NOC:VLSI Physical Design

Subject Co-ordinator - Prof. Indranil Sengupta

Co-ordinating Institute - IIT - Kharagpur

Sub-Titles - Available / Unavailable | MP3 Audio Lectures - Available / Unavailable

Lecture 1 - Introduction  
Lecture 2 - Design Representation  
Lecture 3 - VLSI Design Styles - Part 1  
Lecture 4 - VLSI Design Styles - Part 2  
Lecture 5 - VLSI Physical Design Automation - Part 1  
Lecture 6 - VLSI Physical Design Automation - Part 2  
Lecture 7 - Partitioning  
Lecture 8 - Floor planning  
Lecture 9 - Floor planning Algorithms  
Lecture 10 - Pin Assignment  
Lecture 11 - Placement - Part 1  
Lecture 12 - Placement - Part 2  
Lecture 13 - Placement - Part 3  
Lecture 14 - Placement - Part 4  
Lecture 15 - Grid Routing - Part 1  
Lecture 16 - Grid Routing - Part 2  
Lecture 17 - Grid Routing - Part 3  
Lecture 18 - Global Routing - Part 1  
Lecture 19 - Global Routing - Part 2  
Lecture 20 - Detailed Routing - Part 1  
Lecture 21 - Detailed Routing - Part 2  
Lecture 22 - Detailed Routing - Part 3  
Lecture 23 - Detailed Routing - Part 4  
Lecture 24 - Clock Design - Part 1  
Lecture 25 - Clock Design - Part 2  
Lecture 26 - Clock Design - Part 3  
Lecture 27 - Clock Network Synthesis - Part 1  
Lecture 28 - Clock Network Synthesis - Part 2  
Lecture 29 - Clock Network Synthesis - Part 3

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- Lecture 30 - Clock Network Synthesis - Part 4
- Lecture 31 - Power and Ground Routing
- Lecture 32 - Time Closure - Part 1
- Lecture 33 - Time Closure - Part 2
- Lecture 34 - Time Closure - Part 3
- Lecture 35 - Time Closure - Part 4
- Lecture 36 - Time Closure - Part 5
- Lecture 37 - Timing Driven Placement
- Lecture 38 - Timing Driven Routing
- Lecture 39 - Physical Synthesis - Part 1
- Lecture 40 - Physical Synthesis - Part 2
- Lecture 41 - Performance-Driven Design Flow
- Lecture 42 - Miscellaneous Approaches to Timing Optimization
- Lecture 43 - Interconnect Modeling - Part 1
- Lecture 44 - Interconnect Modeling - Part 2
- Lecture 45 - Design Rule Check
- Lecture 46 - Layout Compaction - Part 1
- Lecture 47 - Layout Compaction - Part 2
- Lecture 48
- Lecture 49
- Lecture 50
- Lecture 51
- Lecture 52
- Lecture 53 - Test Pattern Generation
- Lecture 54 - Design for Testability
- Lecture 55 - Boundary Scan Standard
- Lecture 56 - Built-in Self-Test - Part 1
- Lecture 57 - Built-in Self-Test - Part 2
- Lecture 58 - Low Power VLSI Design
- Lecture 59 - Techniques to Reduce Power
- Lecture 60 - Gate Level Design for Low Power - Part 1
- Lecture 61 - Gate Level Design for Low Power - Part 2
- Lecture 62 - Other Low Power Design Techniques
- Lecture 63 - Algorithmic Level Techniques for Low Power Design
- Lecture 64 - Summarization of the Course